UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,880	03/04/2002	Mayan Moudgill	YOR9-2001-0204US1 (8728-	6258

22150 7590 02/23/2005

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,880	MOUDGILL, MAYAN	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-16,18 and 19* is/are pending in the application.

4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 10, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Gageldonk et al. (U.S. Patent Application Publication No. 2002/0042909) (hereafter referred to as Van Gageldonk et al.'909).

Referring to claim 1, Van Gageldonk et al.'909, as claimed, a microprocessor for processing instructions (see Fig. 1), comprising: a plurality of clusters (UC1, UC2, …, UC7, see Fig. 1) for receiving the instructions, each of the clusters having a

plurality of functional units (see Paragraph 0023, line 24-last line, such as function units: ALU1, L/S1, BU1, MUL1 in UC1) for executing the instructions; and a plurality of register sub-files (RF1, RF2, RF3, and RF4, see Fig. 1) each having a plurality of registers (certainly existing in each Register sub-files RF1, RF2, RF3, and RF4, see Fig. 1) for storing data for executing the instructions, wherein each of the clusters is associated with corresponding one of the register sub-files (see Fig. 1, such as UC1 associated with RF1, UC2 associated with RF1, UC3 associated with RF2, UC4 associated with RF2, UC5 associated with RF3) so that an instruction dispatched (by such as instruction queue or instruction issuing unit in the Van Gageldonk et al.'909's system) to a cluster is executed by accessing registers in a register sub-file (RF1, RF2, RF3, and RF4, see Fig. 1) associated with the cluster to which the instruction is dispatched, and wherein each of the register sub-files has one write port (result output port, see Paragraph 0023, lines 1-7, regarding one result output port for each of the cluster UC1 to UC7, see also Fig. 1) to which a corresponding cluster sends data to be written into registers in a register sub-file (RF1, RF2, RF3, and RF4, see Fig. 1) associated with the corresponding cluster (see Fig. 1, such as

UC1 associated with RF1, UC2 associated with RF1, UC3 associated with RF2, UC4 associated with RF2, UC5 associated with RF3).

Referring to claim 10, Van Gageldonk et al.'909 discloses, as clamed, a system for processing an instruction in a microprocessor, comprising: at least one cluster (UC1, UC2, …, UC7, see Fig. 1) having at least one functional unit (see Paragraph 0023, line 24-last line, such as function units: ALU1, L/S1, BU1, MUL1 in UC1; and BiQ function unit in UC7) for executing the instruction; and at least one register file (RF4, see Fig. 1) having a predetermined number of physical registers (certainly existing in RF4, see Fig. 1) to and from which data is write and read in accordance with the instruction, wherein the at least one register file (RF4, see Fig. 1) has one write port (result output port, see Paragraph 0023, lines 1-7, regarding one result output port for each of the cluster UC1 to UC7, see also Fig. 1) to which an output of the at least one cluster (UC7, see Fig. 1) is connected, and data write operation in accordance with the instruction executed by the at least one functional unit (BiQ function unit in UC7) is performed by accessing the physical registers of the at least one register file (RF4, see Fig. 1).

As to claim 3, Van Gageldonk et al.'909 also discloses: the register sub-files (RF1, and RF2 see Fig. 1) each have a

same number of registers (see Fig. 1, RF1 and RF2 have the same number of registers).

As to claim 11, Van Gageldonk et al.'909 also discloses: the at least one cluster includes multiple functional units (see Paragraph 0023, line 24-last line, such as function units: ALU1, L/S1, BU1, MUL1 in UC1) each for executing different instructions.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-9, 12-16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Gageldonk et al.'909 in view of Levy et al. (U.S. Patent Application Publication No. 2001/0004755) (hereafter referred to as Levy et al.'755).

Referring to independent claim 15, Van Gageldonk et al.'909, as claimed, a method for processing instructions in a microprocessor, comprising the steps of: providing clusters (UC1, UC2, …, UC7, see Fig. 1) each having functional units (see Paragraph 0023, line 24-last line, such as function units: ALU1, L/S1, BU1, MUL1 in UC1) for executing the instructions; dividing a register file into a plurality of register sub-files (RF1, RF2, RF3, and RF4, see Fig. 1) each having registers (certainly existing in each sub-files RF1, RF2, RF3, and RF4, see Fig. 1) to store data for executing the instructions; associating each of the register sub-files (RF1, RF2, RF3, and RF4, see Fig. 1) with corresponding one of the clusters (UC1, UC2, …, UC7, see Fig. 1);

Providing one write port (result output port, see Paragraph 0023, lines 1-7, regarding one result output port for each of the cluster UC1 to UC7, see also Fig. 1) for each of the register sub-files so that a cluster associated with a register

sub-file sends data to be written to a write port of the register sub-file;

selecting (by Van Gageldonk et al.'909's system based on such as the operations defined by the opcode of the instruction) a cluster to which an instruction is dispatched; and dispatching the instruction (by such as instruction queue or instruction issuing unit in the Van Gageldonk et al.'909's system) to the selected cluster (UC1, UC2, …, UC7, see Fig. 1) wherein the instruction is executed by functional units (see Paragraph 0023, line 24-last line, such as function units: ALU1, L/S1, BU1, MUL1 in UC1).

Van Gageldonk et al.'909 discloses the claimed invention except for: a register-renaming unit for renaming target registers in an instruction with registers in a register sub-file associated with a cluster to which the instruction is dispatched (claim 4); the register-renaming unit identifies a register to be used to store a value named by a target register in the instruction (claims 5 and 18); issue-queue units each of which is associated with a corresponding one of the clusters, an issue-queue unit holding instruction renamed by the register-renaming unit until the renamed instruction is issued to be executed in a cluster associated with the issue-queue unit (claims 6, 14 and 19); each of the issue-queue units holds state

identifying which instructions need to be executed (claim 7); renaming target registers in the instruction with registers in a register sub-file associated with the selected cluster (claims 12 and 15); the architected registers are target registers in which a result of the instruction is stored (claim 13).

Levy et al.'755 shows, a register-renaming unit (Register Handler 28, see Fig. 9) for renaming target registers in an instruction (see Fig. 9 changing from instructions to instructions) with registers in a register sub-file associated with a cluster to which the instruction is dispatched; the register-renaming unit (Register Handler 28, see Fig. 9) identifies a register to be used to store a value named by a target register in the instruction (see Fig. 9 changing from instructions to instructions); issue-queue units (see FP instruction queue 32; and Integer instruction queue 30 in Fig. 1) each of which is associated with a corresponding one of the clusters, an issue-queue unit (see FP instruction queue 32; or Integer instruction queue 30 in Fig. 1) holding instruction renamed by the register-renaming unit (Register Handler 28, see Fig. 9) until the renamed instruction is issued to be executed (see EXEC stage 54 in Fig. 2) in a cluster associated with the issue-queue unit (Register Handler 28, see Fig. 9); each of the issue-queue units (Register Handler 28, see Fig. 9) holds state

(certainly existing in order to control the instruction issue) identifying which instructions need to be executed; renaming target registers (by Register Handler 28, see Fig. 9) in the instruction with registers (108 see Fig. 9 and Paragraph [0060] on page 5) in a register sub-file associated with the selected cluster; the architected registers (such as Ar1 and AR2 in Fig. 9) are target registers in which a result of the instruction is stored.

Van Gageldonk et al.'909's system does not explicitly show using renaming registers. Register reference delay is a bottlebeck in the system using a lot of registers inside the register files. Using the renaming registers for dynamic instruction sheduling and dynamic allocating the registers will significantly improve the Van Gageldonk et al.'909's system performance.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Van Gageldonk et al.'909's system to comprise a register-renaming unit for renaming target registers in an instruction with registers in a register sub-file associated with a cluster to which the instruction is dispatched; the register-renaming unit identifies a register to be used to store a value named by a target register in the instruction; issue-queue units each of

which is associated with a corresponding one of the clusters, an issue-queue unit holding instruction renamed by the register-renaming unit until the renamed instruction is issued to be executed in a cluster associated with the issue-queue unit; each of the issue-queue units holds state identifying which instructions need to be executed; renaming target registers in the instruction with registers in a register sub-file associated with the selected cluster; and dispatching the instruction to the selected cluster wherein the instruction is executed by functional units; the architected registers are target registers in which a result of the instruction is stored, as taught by Levy et al.'755, in order to facilitate dynamic instruction scheduling for reorder or parallel operations to increase the processor performance for the Van Gageldonk et al.'909's system (see paragraph 0003, lines 1-3, and lines 8-11).

As to claim 8, Van Gageldonk et al.'909 also discloses: an instruction dispatch mechanism (comprising such as instruction queue or instruction issuing unit in the Van Gageldonk et al.'909's system) for determining which of the clusters each instruction is dispatched to.

As to claim 9, Van Gageldonk et al.'909 also discloses: the instruction dispatch mechanism (comprising such as instruction queue or instruction issuing unit in the Van Gageldonk et

al.'909's system) controls the issue-queue units to determine which of the instructions need to be executed (based on such as the operations defined by the opcode of the instruction).

As to claim 16, and as set forth in claim 3, Van Gageldonk et al.'909 also discloses: the register sub-files (RF1, and RF2 see Fig. 1) each have a same number of registers (see Fig. 1, RF1 and RF2 have the same number of registers).

Response to Arguments

5. Applicant's arguments mailed 12/23/04 have been considered but are moot in view of the new ground(s) of rejection. Van Gageldonk et al.'909 and Levy et al.'755 teach the claimed invention.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful,

the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

7. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
February 22, 2005